REMARKS

This amendment is responsive to the Office Action of February 18, 2009. Reconsideration and allowance of **claims 2, 3, 5-15, 18, and 20-22** are requested.

The Office Action

Claims 2-3, 5-7, 13, and 20-22 were rejected under 35 U.S.C. 112, first paragraph.

Claims 2-3, 5-7, 13, and 20-22 were rejected under 35 U.S.C. 112, second paragraph.

Claims 2-3, 5, 7, 13, and 20-21 were rejected under 35 U.S.C. 103(a) over Wu et al. (US Patent No. 6,909,162) in view of Netzer et al. (US Patent No. 6,177,293).

Claims 6 and 22 were rejected under 35 U.S.C. 103(a) over Wu et al. in view of Kimura (US Patent No. 5,214,683).

Claim 8 does not stand rejected and is understood to contain allowable subject matter.

Drawings

The Office Action asserts that Fig. 2 is merely a circuit diagram of the claimed invention, wherein the drawn length of the source follower transistor gate is not indicative as to its actual length and such drawing does not provide any structural relationship between the length of the gate and the doped regions in the semiconductor substrate. It is respectfully submitted that Fig. 2 does show the gate of the reset transistor having a length which is longer the length of the date of the source follower transistor. The specification describes Fig. 2 as an electrical circuit of a three transistor cell. It is clearly shown in the drawing that the gate of the source follower transistor is shorter than the gate of the reset transistor. Furthermore, the components of circuit diagrams often have symbols that represent a feature of the physical construction of the device. It is respectfully submitted that a length of gate of a transistor can be clearly shown in a symbol of transistor in a circuit diagram.

In an attempt to advance prosecution, a Replacement Sheet for Sheet 9 of the drawings is enclosed. In the Replacement Sheet, Figure 13 has been added to

show a cross sectional view of the gate of the reset transistor having a length which is longer than the length of the gate of the source follower transistor as suggested by Examiner.

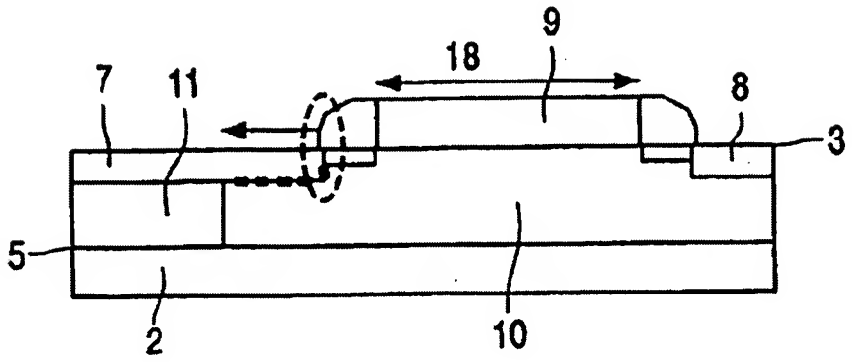
Background

The present application is directed to an image sensor comprising a semiconductor body having a first conductivity type and a surface provided with a number of cells. The cells comprise photosensitive elements and reset transistors. The reset transistors comprise a source region, a drain region, and a gate region, the source region and drain region having a second conductivity type. The source region of the reset transistor is electrically connected to the photosensitive element of the cell.

The above description of the present application is presented to the Examiner as background information to assist the Examiner in understanding the application. The above description is not used to limit the claims in any way.

35 U.S.C. §112 1st Paragraph

The Office Action asserts that the "gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region" is not supported in the specification. It is respectfully submitted that Fig. 4 and page 8 line 23 through page 9 line 33 of the specification supports such a limitation. More specifically, as show in a modified Fig. 4b below, the area within the dashed circle supports the limitation of the gate region (9) overlapping the source region (7) such that *a portion* of the source region (7) is sandwiched between the gate region (9) and the well region (10).



Moreover, moving the gate as shown by the arrow and described on page 9, lines 8 and 9 increases this overlap of the source (7) by the gate (9).

The Office Action also asserts that "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor" is not supported in the specification. It is respectfully submitted that Fig. 13 and page 4 line 14 through page 4 line 22 of the specification supports such a limitation.

35 U.S.C. §112 2nd Paragraph

The Office Action asserts that it is unclear how a two dimensional element (surface) can be provided with three dimensional elements (number of elements). The surface of the semiconductor body is being provided with a number of cells as described in Fig. 1 and page 7 lines 19-30 of the specification. More specifically, the image sensor comprises a number of cells arranged in a two dimensional pattern of horizontal and vertical columns formed along the surface of the semiconductor body.

The Office Action asserts that it is unclear how the well can extend from the surface into the semiconductor body since the well region is located above the surface of the semiconductor body. With reference to Fig. 4b, the well region (10) is located below the surface of the semiconductor body (3) and above the semiconductor (2). This is possible because during the manufacturing process the well region was formed by implanting ions having a first conductor type in the semiconductor body as described on page 12 lines 4-27 of the specification.

The Office Action asserts that is unclear how the source region can extend in a doped region since Fig. 4b depicts the source region being located above the doped region. **Claim 2 and 6** state the source region extends beyond the doped region. The source region does not extend into the doped region but is positioned above the doped region and extends beyond the doped region into the well region.

Additionally, the Office Action asserts that it is unclear as to where the well is present, what is meant by the term "which" and to which well region the Applicant refers, how the well region can extend below itself, which element has a first conductivity type, and whether said gate is the same element as the gate region recited earlier. **Claims 2 and 6** have been amended to address the Examiner's rejections.

The References of Record

Wu et al. is directed to a method for reducing dark current in a photodiode. The photodiode has a semiconductor substrate having a first conductivity type and a well formed in the substrate with a second conductivity type.

Netzer et al. discloses method for forming a CMOS image sensor cell such that stress is minimized in regions surrounding the light sensitive portion of the cell, thereby reducing leakage current and minimizing white spots in CMOS image sensors.

Kimura is directed to a charge detecting device that comprises a source follower amplifier for detecting a variation in a surface potential of a reset transistor. The device allows the setting of a level of the suitable reset pulse in response to a variation in the channel potential of the reset transistor without external circuits for setting reset pulse levels.

The Claims Distinguish Patentably Over the References of Record

Claim 2 is patentable over Wu et al. (US Patent 6,909,162) in view of Netzer et al. (US Patent 6,177,293).

Wu et al. does not disclose wherein the source region extends into the well region and the gate region overlaps the source region such that a portion of the

source region is sandwiched between the gate region and the well region. Wu et al. discloses an image sensor in which the gate ends at the edge of the source region and does not extend beyond the source region. The Office Action asserts that Netzer et al. teaches an image sensor in which the gate region overlaps a source region such that a portion of the source region is sandwiched between the gate and well regions. Examiner refers Applicant to Fig. 2b which discloses a reset transistor comprising a gate and a source region provided on a semiconductor substrate. It is respectfully submitted that Netzer et al. does not discloses a well region and the source region extending into the well region whereby the gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region.

Additionally, the Office Action asserts that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to position a gate region that overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region of Wu et al.'s device. It is respectfully submitted that it would have not been obvious to one of ordinary skill in the art to have sandwiched the source region between the gate region and the well region by positions the gate region so that it overlaps a portion of the source region. Netzer et al. does not teach or suggest a well region or positioning a well region such that the source region is sandwiched between the gate region and the well region. The Examiner has not provided any sufficient reason or evidence that it was conventional in the art to position a gate region that overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region except from using Applicant's invention as a template through a hindsight construction of Applicant's claims.

Accordingly, it is submitted that independent **claim 2** and **claims 3, 5, 7, 13-15, 18, and 20-22** that dependent therefrom distinguish patentably and unobviously over the references of record.

Claim 18, which depends from **claim 2**, is fully supported by the elected species. In the prior amendment, independent **claim 4** was cancelled and **claim 18** was amended to depend from **claim 2**. Because **claim 18** was only grouped in a non-

elected specifies originally, the amendment of **claim 18** changed it from a non-elected to an elected species claim. This amending of **claim 18** is the equivalent of **claim 18** and adding a new claim that is identical to amended **claim 18**.

Claim 6 is patentable over Wu et al. in view of Kimura (US Patent 5,214,683).

Wu et al. does not discloses wherein a source follower transistor is present having a gate connected to the source region of the reset transistor, a gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor. The Office Action asserts that Kimura teaches that the length of the gate of the reset transistor is greater than the length of the gate of the source follower transistor. The Examiner refers Applicant to Fig. 1 which discloses a source follower transistor that is connected to a gate to the source of a reset transistor of an image sensor. Kimura does not suggest or teach that the length of the gate of the reset transistor is greater than the length of the source follower transistor. It is respectfully submitted that Kimura does not disclose a gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor.

Additionally, the Office Action asserts that it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to use a source follower transistor having a gate connected to the source of the reset transistor, wherein the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor, in order to improve the characteristics of Wu et al's device. It is respectfully submitted that that it would have not been obvious to one of ordinary skill in the art to have made the gate of the reset transistor longer than the gate of the source follower transistor. Neither Kimura nor Wu et al. teach or suggest using a gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor. The Examiner has not provided any sufficient reason or evidence that it was conventional in the art to use a gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor except from using Applicant's invention as a template through a hindsight construction of Applicant's claims.

Accordingly it is submitted that **claim 6** distinguishes patentably and unobviously over the references of record.

CONCLUSION

For the reasons set forth above, it is submitted that all claims are not anticipated by and distinguish patentably and unobviously over the references of record. An early allowance of all claims is requested.

Respectfully submitted,

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